

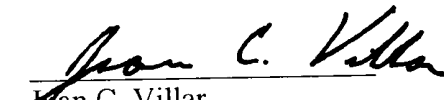
REMARKS

Claim 1 is amended to correspond to the embodiment shown in Figure 1J, namely a dual damascene structure each conductor completely encased in a liner layer.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,

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MARKED UP VERSION OF CLAIMS AMENDMENTS:

Please amend claim 1 as follows:

1. (four times amended) An integrated circuit comprising:

a dielectric layer formed over a substrate;

a first damascene structure in the dielectric layer, the first damascene structure comprising a bottom surface and first and second sidewalls;

a first conductor located in the damascene structure, the conductor comprising a conductive material;[ and]

a first liner layer lining the bottom surface and sidewalls of the first damascene structure and encapsulating the first conductor by contacting a top surface of the first conductor, the liner layer imparts a random grain orientation in the conductive material of the first conductor to improve electromigration lifetime of the first conductor;

a second damascene structure in the dielectric layer, the second damascene structure comprising a bottom surface and second and second sidewalls and disposed above said first damascene structure;

a second conductor located in the damascene structure, the conductor comprising a conductive material;[ and]

a second liner layer lining the bottom surface and sidewalls of the second damascene structure and encapsulating the second conductor by contacting a top surface of the second conductor, the liner layer imparts a random grain orientation in the conductive material of the second conductor to improve electromigration lifetime of the second conductor; and

wherein said second liner layer is in contact with said first liner layer.